

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

1-38. (Canceled)

1           39. (Currently amended): ~~A device according to the 38~~ A device for  
2 controlling a display on a display panel on which a plurality of data lines and a plurality of  
3 scanning lines are arranged in a matrix, the device comprising:  
4           a first generator for generating an original clock signal;  
5           a memory for storing display data received from an external device;  
6           a register for setting a division ratio of the original clock signal and the number of  
7 clocks of a reference clock signal per a scanning period and a number of active lines of the  
8 display panel, all of which being received from the external device;  
9           a second generator for dividing the original clock signal by the division ratio to  
10 generate the reference clock, to thereby generate a line pulse synchronized with the scanning  
11 period and a frame pulse synchronized with a frame period; and  
12           a data line driver for reading out display data from the memory according to the  
13 line pulse and the frame pulse, for converting the display data into a driving voltage to be  
14 provided to the display panel,  
15           wherein the ~~data~~ data line driver reads out the display data line by line from an  
16 address on the memory according to the line pulse, the address corresponding to a top line of the  
17 display panel, and repeats the readout of the display data by using the address corresponding to  
18 the top line of the display panel according to the frame pulse.

1           40.     (Currently amended): ~~A device of according to the 38, the device further~~  
2 ~~comprising~~ A device for controlling a display on a display panel on which a plurality of data  
3 lines and a plurality of scanning lines are arranged in a matrix, the device comprising:  
4                 a first generator for generating an original clock signal;  
5                 a memory for storing display data received from an external device;  
6                 a register for setting a division ratio of the original clock signal and the number of  
7 clocks of a reference clock signal per a scanning period and a number of active lines of the  
8 display panel, all of which being received from the external device;  
9                 a second generator for dividing the original clock signal by the division ratio to  
10 generate the reference clock, to thereby generate a line pulse synchronized with the scanning  
11 period and a frame pulse synchronized with a frame period;  
12                 a data line driver for reading out display data from the memory according to the  
13 line pulse and the frame pulse, for converting the display data into a driving voltage to be  
14 provided to the display panel; and  
15                 a scanning line driver for outputting a selecting voltage and a non-selecting  
16 voltage to the scanning lines on the display panel according to the line pulse and the frame pulse.

41-49. (Canceled)

1           50.     (Currently amended): The device of according to claim[[38]] 39, w herein  
2 the second generator generates the line pulse and the frame pulse from the reference clock based  
3 on the number of clock of the reference clock signal per the scanning period and the number of  
4 the active lines of the display panel.

1           51.     (Currently amended): The device of according to claim[[38]] 39, wherein  
2 a frame frequency of the frame pulse is determined from the division ratio of the original clock  
3 signal, the number of clock of the reference clock signal per the scanning period, and the number  
4 of the active lines of the display panel.

1                   52.     (Currently amended): A device of according to the claim[[38]] 39,  
2     wherein the frame frequency of the frame pulse is adjustable by at least one of the division ratio  
3     of the original clock signal, the number of clock of the reference clock signal per the scanning  
4     period, and the number of the active lines of the display panel to be set in the register from the  
5     external device.

1                   53.     (Currently amended): A device of according to the claim[[38]] 39,  
2     wherein the number of clock of the reference clock signal per the scanning period is an integer.

1                   54.     (New): A device of according to claim 40, wherein the second generator  
2     generates the line pulse and the frame pulse from the reference clock based on the number of  
3     clock of the reference clock signal per the scanning period and the number of the active lines of  
4     the display panel.

1                   55.     (New): A device of according to claim 40, wherein a frame frequency of  
2     the frame pulse is determined from the division ratio of the original clock signal, the number of  
3     clock of the reference clock signal per the scanning period, and the number of the active lines of  
4     the display panel.

1                   56.     (New): A device of according to the claim 40, wherein the frame  
2     frequency of the frame pulse is adjustable by at least one of the division ratio of the original  
3     clock signal, the number of clock of the reference clock signal per the scanning period, and the  
4     number of the active lines of the display panel to be set in the register from the external device.

1                   57.     (New): A display controller used for a display panel on which a plurality  
2     of data lines and a plurality of scanning lines are arranged in a matrix, the display controller  
3     comprising:

4                   a first generator for generating an original clock signal;  
5                   a memory for storing display data received from an external device to the display  
6     controller;

7 a register for setting a division ratio of the original clock signal, the number of  
8 clocks of a reference clock signal per a scanning period, and a number of active lines of the  
9 display panel, all of which can be changed by the external device;

10 a second generator for dividing the original clock signal by the division ratio to  
11 generate the reference clock, to thereby generate a line pulse synchronized with the scanning  
12 period and a frame pulse synchronized with a frame period; and

13 a data line driver for converting the display data from the memory into a driving  
14 voltage to be provided to the display panel,

15 wherein the data line driver reads out the display data from an address on the  
16 memory according to the line pulse, the address corresponding to a top line of the display panel,  
17 and repeats the readout of the display data by using the address corresponding to the top line of  
18 the display panel according to the frame pulse.

1 58. (New): A display controller according to the claim 57, the display  
2 controller further comprising a scanning line driver for outputting a selecting voltage and a non-  
3 selecting voltage to the scanning lines on the display panel.

1 59. (New): A display controller according to the claim 58, the display  
2 controller is one LSI chip.

1 60. (New): A display controller according to the claim 57, wherein the  
2 display controller can operate in a partial display mode or a low power consumption mode of the  
3 display panel.

1 61. (New): A display controller according to the claim 57, wherein the  
2 display controller is incorporated into a cellular phone system.

1                   62.     (New): A display controller used for a display panel on which a plurality  
2 of data lines and a plurality of scanning lines are arranged in a matrix, the display controller  
3 comprising:  
4                   a first generator for generating an original clock signal;  
5                   a memory for storing display data received from an external device to the display  
6 controller;  
7                   a register for setting a division ratio of the original clock signal, a number of clock  
8 of a reference clock signal per a scanning period and a number of active lines of the display  
9 panel, all of which can be changed by the external device;  
10                  a second generator for dividing the original clock signal by the division ratio to  
11 generate the reference clock, to thereby generate a line pulse synchronized with the scanning  
12 period and a frame pulse synchronized with a frame period; and  
13                  a data line driver for converting the display data from the memory into a driving  
14 voltage to be provided to the display panel; and  
15                  a scanning line driver for outputting a selecting voltage and a non-selecting  
16 voltage to the scanning lines on the display panel according to the line pulse and the frame pulse.

1                   63.     (New): A display controller according to the claim 62, the display  
2 controller is one LSI chip.

1                   64.     (New): A display controller according to the claim 62, wherein the  
2 display controller can operate in a partial display mode or a low power consumption mode of the  
3 display panel.

1                   65.     (New): A display controller according to the claim 62, wherein the  
2 display controller is incorporated into a cellular phone system.